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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,892	04/12/2001	Takehisa Yamaguchi	205975US2	1675

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EXAMINER	
NGUYEN, HOAN C	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,892	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 11 objected to because of the following informalities: the limitation "depositing a conducting film serving as source/drain electrodes on said insulating film" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 5-10 and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Takashi (JP1267617).

In regard to claims 1, 2, Nakazawa teaches (Fig. 1) a liquid crystal display comprising:

- a gate electrode lIne 106 including a gate electrode formed on an insulating substrate;
- a source electrode line 108 including a source electrode103 intersected with said gate electrode line 106 via an insulating film (gate insulating film 105);

- a thin film transistor located in a vicinity of a portion in which said gate electrode line is intersected with said source electrode line;
- two drain electrode lines 102, each including two drain electrodes in said thin film transistor, said drain electrode line being connected with a pixel electrode 107;

wherein

- said thin film transistor includes said two drain electrode lines located on both sides of said source electrode; said two drain electrodes are formed at a place where each end portion of said two drain electrode lines opposed to said source electrode is superposed with said gate electrode line.
- an area of a region where said gate electrode line 106 is superposed with one of said two drain electrode lines is substantially identical to an area of a region where said gate line is superposed with the other one of said two drain electrode lines as shown in Fig. 1b according to claim 2.
- a length of a region in a channel lengthwise direction of said thin film transistor where said gate electrode line is superposed with one of said two drain electrodes is substantially identical to a length 109 of a region in a channel lengthwise direction of said thin film transistor where said gate electrode line is superposed with the other one of said two drain electrode lines according to claim 3,
- said drain electrode is formed in whole part of one end of said drain electrode line in a channel widthwise direction where said drain electrode line is superposed with said gate electrode line according to claim 5;

- said drain electrode is formed at a portion where a part of one end of said drain electrode line in the channel widthwise direction opposed to said source electrode is superposed with said gate electrode line on both sides of said source electrode according to claim 6;
- a lead portion 103 of said source electrode line 108 extended to said source electrode 103 from said source electrode line is provided with a semiconductor film situated below said gate electrode line via an insulating film in reference to the insulating substrate according to claim 7;
- a lead portion of said source electrode line extended to said source electrode from said source electrode line is provided with a semiconductor film 105; said semiconductor film being situated above said lead portion 103 of said source electrode according to claim 8;
- said two drain electrodes opposed to said source electrode on both sides of said source electrode are connected with each other in the region between said two drain electrode lines and said pixel electrode, said drain electrodes being connected with said pixel electrode by a single part of said drain electrodes according to claim 9.
- said drain electrode line is formed of a same film as that of said pixel electrode according to claim 10;

In regard to claims 12 and 13, Nakazawa teaches (Fig. 1b) a method for manufacturing a liquid crystal display comprising steps of

- depositing a conductive film on an insulating substrate serving as source/drain electrodes 102/103;
- subjecting said deposited conductive film to patterning in such a manner that two drain electrodes are formed in a portion where each part of the two drain electrode lines extending in a channel lengthwise direction is superposed with a gate electrode line, said drain electrode lines being opposed to said source electrode on both side surfaces;
- forming a semiconductor film 104 on said source/drain electrodes;
- forming an insulating film 105 in such a manner as to cover said semiconductor film;
- forming a gate electrode pattern 106 on said insulating film
- forming a pixel electrode pattern 107 connected with said drain electrode, wherein said drain electrode is formed in said step of forming said pixel electrode pattern according to claim 13.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US6191831B1).

Kim et al. teach (Fig. 4) a method for manufacturing a liquid crystal display comprising steps of

- forming a gate electrode line pattern 22-1 on an insulating substrate 20;
- forming a semiconductor film 26-1 covering said gate electrode line;
- depositing a conductive film serving as source/drain electrodes 24b-1/24b-2 on said (insulating?) semiconductor film;
- subjecting said deposited conductive film to patterning in such a manner that two drain electrodes 24b-1 are formed in a portion where each end of two drain electrodes opposed to said source electrode 24b-a is superposed in a channel lengthwise direction with said gate electrode line on both sides of said source electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi (JP1267617) as applied to claims 1-3 above.

It is conventional in the thin film transistor manufacture that a length of the area in the channel lengthwise direction is such a length as to prevent a current characteristics from degradation in a thin film transistor.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Muto (US4902638) discloses a thin film transistor comprising a gate electrode, at east two drain electrodes connected to the picture element displaying electrode, a source bus line, a plurality of source electrodes connected to the source bus line, which applies a voltage to the source electrodes.

Okabe et al. (US4894690) disclose a thin film transistor comprising the two source electrodes formed of aluminum simultaneously with the source bus 3 and the two drain electrodes.

Komaki (JP2193122) discloses a thin film transistor panel with two thin film transistors, one on gate line and one on the date line.

Takashi (JP2079476) discloses a film type transistor with two drain electrodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (703) 306-0472. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SIKES L WILLIAM can be reached on (703) 308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

746-8178 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0530.

HOAN C. NGUYEN
Examiner
Art Unit 2871

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September 10, 2002

TOAN TON
PRIMARY EXAMINER